AMENDMENTS TO THE SPECIFICATION:

At page 1, please replace paragraph [0003] as indicated:

[0003] It is typical for oscillators that in addition to the actual clock signal they also produce different harmonic frequencies. This is a feature of all oscillators. Harmonics are ~~multiplies~~multiples of the actual clock signal frequency. Harmonics caused by clock signals may cause problems in sensitive radio frequency parts in radio devices, such as transceivers in cellular systems. For example, in transceivers of GSM cellular system, VCTCXO Oscillators are widely used (as 13MHz or 26MHz reference clocks, for example). Harmonics arising from the clock signal can be seen as reduced receiver sensitivity on some radio channels or as interference peaks in the receiver band noise spectrum.

At page 3, please replace paragraph [0016] as indicated:

[0016] Figure 1 illustrates square waves with different pulse widths. Clock signals are typically generated as square waves. A square wave 100 has two cycles: a duty cycle 102 when the pulse signal is up and a rest cycle 104 when the pulse signal is down. In the square wave 100 both cycles are of the same length. It can thus be said that the square wave 100 has a duty cycle of 0.5. In a square wave 106 the duty cycle 102 is shorter compared with the rest cycle 104. The duty cycle of the square wave [[104]]106 is in this case smaller than 0.5. Respectively, as in the square wave [[106]]108 the duty cycle 102 is longer compared with the rest cycle 104, the duty cycle of the square wave [[104]]108 is greater than 0.5.

At page 4, please replace paragraph [0022] as indicated:

[0022] From the converter 328 the digital signals are forwarded to a digital controller 334. The controller further processes the received signals. The controller also controls the operation of the receiver. The apparatus is able to communicate on different radio channels. The controller [[328]]334 may control the operation of the voltage-controlled oscillator via

the phase locked loop in such a way that the desired radio channel frequency is down-converted in the mixers 314, 316. The controller may be realized using a digital signal processor, a general processor or discrete components, and suitable software.

At page 4, please replace paragraph [0025] as indicated:

[0025] In an embodiment of the invention the controller [[338]]334 of the apparatus controls the pulse width of the clock signal. The digital control signal 348 of the converter is converted into an analog form in a D/A-converter 350 and the output of the converter 350 is connected to the buffer 344.

At pages 4-5, please replace paragraph [0026] as indicated:

[0026] Figure 4 illustrates an example of the buffer control, where the pulse width is implemented by changing an offset in the buffer input. The output signal 342 from the oscillator 340 is taken to the buffer 344 as an input. The D/A-converter 350 receives a control signal 348 from the controller. The signal level indicated by the signal corresponds to an offset voltage of the buffer. The D/A converter outputs an analogue offset signal in a differential form 400, 402 to the buffer [[342]]344. The differential form comprises the required offset voltage O_o in a positive and negative form ($+O_o$ and $-O_o$). The buffer converts the sinusoidal oscillator signal 342 into a square wave 346.

At page 5, please replace paragraph [0029] as indicated:

[0029] The digitized signal [[form]]from the output of the converter 328 is taken into the base band controller 334, which is arranged to detect interference peaks in the signal in step 502. On the basis of the found interference peaks the controller generates 504 a control signal 348 for the pulse width control. The signal is then converted to an analog signal in

the converter 350 and passed to the clock signal buffer 344 where the pulse width of the signal is adjusted 506 on the basis of the signal.